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Retargetable Generation of Code Selectors from HDL Processor.. - Leupers, Marwedel (1997) (Correct) (9 citations)
Retargetable Generation of Code Selectors from HDL
In contrast to previous work, our retargetable compiler Record does not require toolspecific modelling
Retargetable Generation of Code Selectors from HDL Processor Models Rainer
ls12-www.cs.uni-dortmund.de/publications/papers/1997-edtc.ps.gz

Optimizing ML with Run-Time Code Generation - Leone, Lee (1995) (Correct) (91 citations)
and Todd A. Proebsting. DCG: An efficient, retargetable dynamic code generation system. In Proceedings
We describe the design and implementation of a compiler that automatically translates ordinary programs
Optimizing ML with Run-Time Code Generation Mark Leone Peter Lee December 1995
foxnet.cs.cmu.edu/~petel/papers/staged/mleone-pldi96.ps

Lightweight Run-Time Code Generation - Leone, Lee (1994) (Correct) (34 citations)
and Todd A. Proebsting. DCG: An efficient, retargetable dynamic code generation system. In
strategies developed for a prototype compiler are discussed, and the results of preliminary
Lightweight Run-Time Code Generation Mark Leone Peter Lee Carnegie Mellon
www.cs.cmu.edu/afs/cs.cmu.edu/user/mleone/papers/lw-rtcg.ps

Global Instruction Scheduling In Machine SUIF - Gang Chen (1997) (Correct) (2 citations)
Abstract Machine SUIF is a retargetable compiler backend designed by the HUBE research
Abstract Machine SUIF is a retargetable compiler backend designed by the HUBE research group at
In addition, we propose the use of multiple-path code motions for further avoiding redundant
www.eecs.harvard.edu/machsuif/papers/hpca3.ps

Binary Translation: Static, Dynamic, Retargetable? - Cifuentes, Malhotra (1996) (Correct)
Binary Translation: Static, Dynamic, Retargetable? Cristina Cifuentes Department of Computer
binary or machine code is performed by means of a compiler and a linker (see Figure 1)Linkers have
on the old machine. The transformation of source code to binary or machine code is performed by means of
www.it.uq.edu.au/personal/cristina/icsm96.ps

Solving graph problems with dynamic computation structures - Babb, Frank, Agarwal (1996) (Correct) (18 citations)
MIT, June 1992. 6] D. R. Engler. VCODE: A retargetable, extensible, very fast dynamic code generation
computing fabric. Thus, a virtual wires compiler, coupled with front-end commercial behavioral
(DCS)a compilation technique to produce dynamic code for reconfigurable computing. DCS specializes
ftp.cag.lcs.mit.edu/pub/raw/documents/Babb:SPIE:1996.ps.Z

Verification of Hardware Descriptions by Retargetable Code.. - Nowak, Marwedel (1989) (Correct) (10 citations)
Verification of Hardware Descriptions by Retargetable Code Generation Lothar Nowak Nixdorf Computer
basic idea is the application of a retargetable compiler as verification tool. A retargetable compiler is
of Hardware Descriptions by Retargetable Code Generation Lothar Nowak Nixdorf Computer AG
ls12-www.informatik.uni-dortmund.de/publications/papers/1989-dac.ps.gz

Fortran 90D/HPF Compiler for Distributed Memory.. - Bozkus.. (1993) (Correct) (2 citations)
Fortran 90D/HPF Compiler for Distributed Memory MIMD Computers: Design,
for the compiler are presented which show that the code produced by the compiler is portable, yet
ftp.cis.ufl.edu/pub/faculty/ranka/compiler_sc93.ps.Z

A Design Example Using CASTLE - Plöger, Wilberg (Correct)
[5]8] extends this approach by providing a retargetable code-generation and an instructionset
processor hardware, as well as the corresponding compiler for generating the processor opcode. The main
(ploeger,wilberg)gmd. de Abstract. CASTLE is a codesign platform which provides a number of design

alcatraz.gmd.de:9422/~paul/word/dmm95/dmm95.ps

Experience with a Clustered Parallel Reduction Machine - Beemster, Hartel.. (1993) (Correct) (1 citation)
of the application onto the available hardware. Compilers for imperative languages also use program
analysis on non-flat domains and RISC and VLIW code generation. Parallel jobs are distributed by an
www.wins.uva.nl/pub/computer-systems/functional/reports/FGCS_experience.ps.Z

A BDD-based Frontend for Retargetable Compilers - Leupers, Marwedel (1995) (Correct) (8 citations)
$4.00 c fi1995 IEEE 1 A BDD-based Frontend for Retargetable Compilers Rainer Leupers, Peter Marwedel
IEEE 1 A BDD-based Frontend for Retargetable Compilers Rainer Leupers, Peter Marwedel University of
for DSP processors still do not provide sufficient code quality in case of hard real-time constraints.
ls12-www.cs.uni-dortmund.de/publications/papers/1995-edtc.ps.gz

The Jalapeño Dynamic Optimizing Compiler for Java - Burke, Choi, Fink.. (1999) (Correct) (24 citations)
of the test (such as getfield)6.3 BURS-based Retargetable Code Generation In this section, we address
The Jalape~no Dynamic Optimizing Compiler for Java TM Michael G. Burke Jong-Deok Choi
www.mcs.newpaltz.edu/~hind/papers/grande99.ps

Stack-Based Typed Assembly Language - Morrisett, Crary, Walker, Glew (1998) (Correct) (24 citations)
expressive to serve as a target language for compilers of high-level languages such as ML. That work
compilation, typed assembly language, certified code, polymorphic recursion, stacks. 1 Introduction
reports-archive.adm.cs.cmu.edu/anon/1998/CMU-CS-98-178.ps

RTL Calls Generator - Labarta (1998) (Correct)
for the next period of the project. Contents 1 Compiler Activities Workplan 2 2 Parafrase-2 Initial
ftp.ac.upc.es/pub/reports/CEPBA/1998/UPC-CEPBA-1998-16.ps.Z

Instruction-Set Modelling for ASIP Code Generation - Leupers, Marwedel (1996) (Correct)
in code generation for ASIPs is to develop retargetable compilers in order to permit exploration of
generation for ASIPs is to develop retargetable compilers in order to permit exploration of different
Instruction-Set Modelling for ASIP Code Generation Rainer Leupers, Peter Marwedel
ls12-www.informatik.uni-dortmund.de/publications/papers/1998-vlsi-design.ps.gz

Retargetable Code Generation For Parallel, Pipelined Processor.. - Schenk (1995) (Correct)
1 Retargetable Code Generation For Parallel, Pipelined
behavior of the RT level modules, the proposed compiler maps a source program to the binary code of the
1 Retargetable Code Generation For Parallel, Pipelined Processor
ls12-www.informatik.uni-dortmund.de/publications/papers/1995-kap.ps.gz

An Integrated Compilation and Performance Analysis Environment for .. - Adve (1995) (Correct) (30 citations)
requires a unique degree of integration between compilers and performance analysis tools. Compilers for
vibes.cs.uiuc.edu/Publications/Papers/HPF.ps.gz

Retargetable Code Generation based on Structural Processor.. - Leupers, Marwedel (1998) (Correct) (12 citations)
Boston. Manufactured in The Netherlands. Retargetable Code Generation based on Structural Processor
systems and embedded processors. General-purpose compilers for standard processors are often insufficient,
ls12-www.cs.uni-dortmund.de/publications/papers/1998-daes.ps.gz

Code Composition as an Implementation Language for Compilers - Stichnoth, Gross (1997) (Correct) (6 citations)
Code Composition as an Implementation Language for Compilers James M. Stichnoth and Thomas Gross School of
Code Composition as an Implementation Language for
pecan.srv.cs.cmu.edu/afs/cs.cmu.edu/user/stichnot/public/www/dsl97.ps

A First Implementation of Modular Smalltalk - Holst, Szafron (1993) (Correct)
Smalltalk, object-oriented, programming language, compiler, interpreter, method dispatch, code generation.
parser, object-oriented representation for code fragments and an object-oriented C-code generator,
other languages like assembler. In addition, the generation technique applies to source languages other
menalk.cs.ualberta.ca/pub/TechReports/1993/TR93-07/TR93-07.ps.Z

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Quantum Computing - Shor (1998) (Correct) (7 citations)
of the factoring algorithm, A question that has **generated** much discussion is where the extra power of into consideration. A quantum computer is a **hypothetical machine** based on quantum mechanics. We explain A quantum computer is a **hypothetical machine** based on quantum mechanics. We explain quantum elib.uni-osnabrueck.de/EMIS/journals/DMJDMV/xvol-icm/Fields/../00/Shor.MAN.ps.gz

Approximation in Model-Based Learning - Leonid Kuvayev (1997) (Correct) (2 citations)
of occurrence. When the model is used to **generate hypothetical** next states, one of the previously occurrence. When the model is used to **generate hypothetical** next states, one of the previously observed with function approximation. In Proceedings of the **Machine** Learning Conference. San Francisco, CA: Morgan ftp.cs.umass.edu/pub/anw/pub/kuvayev/kuvayev-sutton-mlshop97.ps

Intuitionistic Deductive Databases And The Polynomial Time.. - Bonner (1997) (Correct) (1 citation)
do not need this assumption, since they can **generate** linear orders on a domain **hypothetically** [6] where one must explore the consequences of **hypothetical** actions and possibilities. To address this ftp.cs.toronto.edu/pub/bonner/papers/hypotheticals/jlp96b.ps

Programmable Active Memories: Reconfigurable Systems.. - Vuillemin, Bertin.. (1996) (Correct) (71 citations)
circuit design. Our emphasis is on large, code-**generated** synchronous systems descriptions no compromise all other existing implementation media. A **hypothetical machine** equipped with a dozen different Gate Array (FPGA) technology, a PAM is a virtual **machine**, controlled by a standard microprocessor, which ftp.digital.com/pub/DEC/PRL/research-articles/VBRSTB941.ps.Z

A Logic for Hypothetical Reasoning - Bonner (1988) (Correct) (2 citations)
A Logic for **Hypothetical** Reasoning Anthony J. Bonner Rutgers ftp.cs.toronto.edu/pub/bonner/papers/hypotheticals/aaai88.ps

Embra: Fast and Flexible Machine Simulation - Witchel, Rosenblum (1996) (Correct) (38 citations)
speed, Embra uses dynamic binary translation to **generate** code sequences which simulate the workload. It Sigmetrics `96 Embra: Fast and Flexible **Machine** Simulation Emmett Witchel Laboratory for Embra models the processors of a MIPS R3000/R4000 **machine** faithfully enough to run a commercial operating hing.lcs.mit.edu/pub/witchel/papers/SIGMetrics96-embra.ps.Z

AutoAdmin "What-if" Index Analysis Utility - Chaudhuri, Narasayya (Correct) (5 citations)
Most modern databases support the ability to **generate** a representative workload for the system by the DBA should have the ability to propose **hypothetical** (what-if"indexes and quantitatively analyze www.math.tau.ac.il/~matias/courses/papers/autoadmin_conf_version.ps

Hypothetical Datalog: Complexity and Expressibility - Bonner (1988) (Correct) (4 citations)
DB is encoded on the input tape, then the **machine generates** an encoding of /DB) on its output tape after **Hypothetical** Datalog: Complexity and Expressibility ftp.cs.toronto.edu/pub/bonner/papers/hypotheticals/icdt88.ps

Generating Efficient Code for Lazy Functional Languages - Smetsers, Nöcker, van.. (1991) (Correct) (20 citations)
lazy functional programming language, code is **generated** for an intermediate abstract **machine**: the ABC code is **generated** for an intermediate abstract **machine**: the ABC **machine**. In this first pass many for an intermediate abstract **machine**: the ABC **machine**. In this first pass many well-known optimisation ftp.cs.kun.nl/pub/CSI/SoftwEng.FunctLang/papers/smes91-codegeneration.ps.gz

A Parallel Workload Model and Its Implications for Processor.. - Allen Downey (1996) (Correct) (26 citations)
used for scientific applications usually do not **generate** jobs that can change cluster sizes dynamically.

with analysis and simulation based on **hypothetical** workloads. Each of the strategies we consider exclusively and run to completion. Many of these **machines** also have an interactive partition that uses www.sdsc.edu/~downey/allocation/csd-96-922.ps.gz

Microprocessor Verification in PVS - A Methodology and Simple.. - Cyrluk (1994) (Correct) (23 citations)
machine amounts to showing that the traces **generated** by the two **machines** are the same relative to exploring a general methodology of verifying state **machine** systems in the PVS verification system. It Is 5 2 The General Methodology 7 2.1 The State **Machines** : www2.csl.sri.com/reports/postscript/csl-93-12.ps.gz

Commutativity Analysis: A New Analysis Framework for.. - Rinard, Diniz (1996) (Correct) (19 citations)
to discover when operations commute (i.e. **generate** the same final result regardless of the order in parallel code running on the Stanford DASH **machine**. These results provide encouraging evidence that parallel code running on the Stanford DASH **machine**. These results indicate that commutativity www.cs.umd.edu/~hollings/cs818z/s99/papers/rinard.pldi96.ps

Compositional Oil Reservoir Simulation in Fortran D: A.. - Kremer, Ramé (1993) (Correct) (4 citations)
the underlying compilation systems are able to **generate** efficient code for the specified parallelism? is written in a style to take advantage of the **machine** characteristics of a vector supercomputer such vector supercomputer such as a Cray. However, this **machine** dependent programming style inhibits many softlib.rice.edu/pub/CRPC-TRs/reports/CRPC-TR93335-S.ps.gz

The YAIL: An Intermediate Language for the Native Compilation.. - Lopes, Costa (1996) (Correct)
the DEC-10 Prolog system, was designed to **generate** DEC-10 assembly code which that could then be which that could then be executed by the target **machine**. The search for portability and simplicity in where compilers **generate** code for abstract **machines** that are then are emulated at run-time. Examples www.ncc.up.pt/~rslopes/papers/jicslp96.ps.gz

Python and Java: The Best of Both Worlds - Hugunin (1997) (Correct) (4 citations)
faults, and the ability to automatically **generate** wrapper code for arbitrary Java libraries. 1. run on any computer that supports a Java virtual **machine**. Unlike ANSI C, which achieves portability enjoys this advantage and will run on any **machine** with a Python interpreter installed the wealth sunsite.informatik.rwth-aachen.de/python/workshops/1997-10/proceedings/hugunin.ps

Manufacturing Cell Design: An Integer Programming Model.. - Joines, Culbreth, King (1996) (Correct) (1 citation)
allow alternative cell configurations to be **generated** and reviewed easily. The following section described by its use of process technology (part/**machine** incidence matrix)be partitioned into part the associated plant equipment be partitioned into **machine** cells. At the highest level, the objective is to www.fmmcenter.ncsu.edu/fac_staff/joines/papers/./papers/iietran.ps.gz

Uniform Random Number Generators for Vector and Parallel Computers - Brent (1992) (Correct) (3 citations)
Poisson, but the algorithms used to **generate** these random numbers almost invariably require a number generators on modern vector and parallel **machines** consider the pros and cons of various popular efficiently on vector processors and parallel **machines**. A proposal regarding initialization of these nimbus.anu.edu.au/pub/Brent/rpb132tr.ps.gz

Programming with Logical Queries, Bulk Updates and Hypothetical.. - Chen (1995) (Correct)
with Logical Queries, Bulk Updates and **Hypothetical** Reasoning Weidong Chen Computer Science and www.seas.smu.edu/~wchen/papers/updates.ps.gz

Consortium - Release Date (Correct)
of this system will hopefully serve as a model to **generate** backends for other **machines**. IMPORTANT 4 5 Using a Back-end in a COSY Compiler 4 6 The **Machine** Specification 4 7 Various levels of intermediate Serve As A Model To **Generate** Backends For Other **Machines**. Important Preliminary Notice: Pagode, Fnc-2 ftp.inria.fr/INRIA/Projects/oscar/FNC-2/publications/pagode.ps.gz

Achieving Coordination through Combining Joint Planning and Joint.. - Weiss (1999) (Correct)
capability to jointly plan, that is, to jointly **generate hypothetical** activity sequences. Second, by to jointly plan, that is, to jointly **generate hypothetical** activity sequences. Second, by endowing the using multiple reinforcement learning agents. **Machine** Learning, 33(2/3)235-262, 1998. Dec95] K.S. wwwbrauer.informatik.tu-muenchen.de/fki-berichte/postscript/fki-232-99.ps.gz